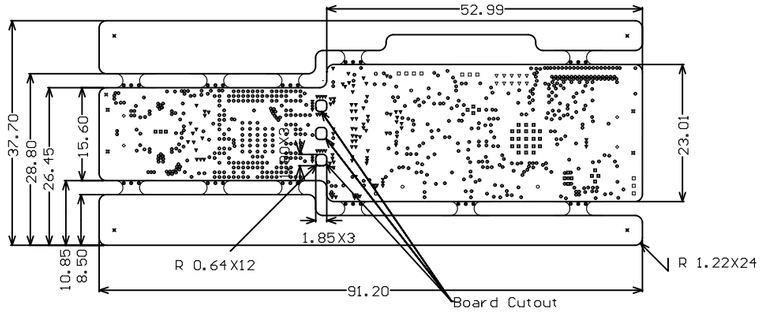
IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	MICROSTRIP	L1,L8	5.50	---	50	L02,L07
02	EDGE COUPLED MICROSTRIP	L8	4.00	4.5	90	L07
03	EDGE COUPLED MICROSTRIP	L8	4.00	7	100	L07
04	EDGE COUPLED MICROSTRIP	L1,L8	4.00	6.1	120	L03,L06
05	STRIPLINE	L3,L6	4.2	---	50	L02/04,L05/07
06	EDGE COUPLED STRIPLINE	L6	4.00	6	90	L05/07
07	EDGE COUPLED STRIPLINE	L3	3.5	8	100	L02/04
08	COPLANAR	L1	12	10	50	L03



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
	36	7.87mil	PTH	Round	Top Layer - Bottom Layer	
	626	8.00mil	PTH	Round	Top Layer - Bottom Layer	
	112	8.00mil	PTH	Round	Top Layer - Bottom Layer	+/-3.00mil
	10	23.62mil	PTH	Round	Top Layer - Bottom Layer	
	4	23.62mil	PTH	Slot	Top Layer - Bottom Layer	
	10	27.56mil	PTH	Round	Top Layer - Bottom Layer	
	33	32.00mil	NPTH	Round	Top Layer - Bottom Layer	
	4	33.47mil	PTH	Round	Top Layer - Bottom Layer	
	1	40.00mil	PTH	Round	Top Layer - Bottom Layer	
	2	40.16mil	NPTH	Round	Top Layer - Bottom Layer	
	1	64.96mil	PTH	Round	Top Layer - Bottom Layer	
	4	88.00mil	NPTH	Round	Top Layer - Bottom Layer	+/-3.00mil
	2	100.00mil	NPTH	Round	Top Layer - Bottom Layer	+/-3.00mil
	845 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.50mil	3.5	
3	Top Layer	Copper	1.37mil		
4	Dielectric1	FR-4 High Tg	3.70mil	4.2	
5	GND1	Copper	2.40mil		
6	Dielectric3	FR-4 High Tg	4.50mil	4.2	
7	Sig1	Copper	1.20mil		
8	Dielectric2	FR-4 High Tg	12.00mil	4.2	
9	PWR1	Copper	2.40mil		
10	Dielectric4	FR-4 High Tg	8.00mil	4.2	
11	PWR2	Copper	2.40mil		
12	Dielectric5	FR-4 High Tg	12.00mil	4.2	
13	Sig2	Copper	1.20mil		
14	Dielectric8	FR-4 High Tg	4.50mil	4.2	
15	GND2	Copper	2.40mil		
16	Dielectric9	FR-4 High Tg	3.70mil	4.2	
17	Bottom Layer	Copper	1.37mil		
18	Bottom Solder	Solder Resist	0.50mil	3.5	
19	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 3.5 MIL
MIN. CLEARANCE: 3.5 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 64 MIL (1.62mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] RED [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[X] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[X] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[X] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: xWR6843AOPEVM
DESIGNED FOR: Public Release
FILE NAME: PROC091F.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC091	REV: F	SVN REV: Not In VersionControl
LAYER NAME = [illegible]	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 11-11-2020 20:24:23	TEXAS INSTRUMENTS	

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ENGINEER:	LAYOUT BY:
Antony/Bala	Mistral Team
SCALE: 1.00	ALTIUM DESIGNER VERSION: 18.0.9.584